



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Thomas, *et al.* Docket No.: 2003 P 54322 US
Serial No.: 10/790,907 Art Unit: 2811
Filed: March 2, 2004 Examiner: TBD
For: Integrated Circuit with Re-Route Layer and Stacked Die Assembly

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Date of Deposit: June 15, 2004

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Information Disclosure Statement (1 page)
PTO/SB/08A & 08B with 17 References Cited (2 pages)
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Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits. In the event a fee is required, please charge any additional amount, or credit any overpayment to Deposit Acct. No.50-1065 of the below mentioned firm.

Pursuant to 37 CFR 1.98(a)(2)(i), as amended, copies of U.S. Patents cited are not being submitted. However, Applicant has included copies of any non-patent literature.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Ira S. Matsil".

June 15, 2004

Date

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PTO/SB/08a (08-03)

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